# An E-Mode GaAs FET Power Amplifier MMIC for GSM Phones

*W. Abey, T. Kawai, I. Okamoto, M. Suzuki, *C. Khandavalli, *W. Kennan, Y. Tateno, M. Nagahara, **M. Takikawa

Fujitsu Ltd
1015 Kamikodanaka, Nakahara-ku, Kawasaki 211, Japan

*Fujitsu Compound Semiconductor, Inc,
2355 Zanker Road, San Jose, CA

**Fujitsu Labs Ltd
10-1 Morinosato-Wakamiya, Atsugi 243-01, Japan

## Abstract

An enhancement-mode three stage GaAs FET power MMIC has been developed for single supply portable applications. The MMIC operates from a 4.8V power supply and provides over 35 dBm output power from 890-915 MHz with more than 35 dB gain and 47% power added efficiency. Power control range is greater than 70dB. Leakage current is 2uA.

## Introduction

The drive to produce smaller, lower cost portable phones has placed demands on transmitter power amplifiers. GaAs FET MMICs have been good candidates for meeting these requirements. They however, traditionally require a dual polarity voltage supply. They may also need a switch between the battery and the drain to eliminate leakage current under non-transmitting conditions. This can lead to higher cost, larger board area and lower efficiency.

This work demonstrates a MMIC PA using enhancement-mode GaAs FETs. Enhancement-mode FETs eliminate the need for a DC-DC converter and sequencing circuitry necessary with depletion-mode devices. The threshold voltage is high enough such that at Vgs=0V the device is pinched off. The leakage current then becomes negligible and a drain switch can be eliminated.

## Device

Enhancement-mode FETs have been reported in the literature [1]-[3]. A new enhancement-mode FET has been developed for power amplifier applications. A trade off between high power density and low leakage current was made to create a device with optimum performance.

A discrete FET with Lg=0.6um and Wg=6mm has, at 900 Mhz, a power added efficiency of 71% and Psat of 27dBm at Vds=4.8V. The linear gain under power matched condition is 18 dB and leakage current is less than 0.2 uA. The

0-7803-4603-6/97/$5.00 (c) IEEE

efficiency and gain are comparable to conventional depletion-mode power FET performance.

## Design

The three stage MMIC chip layout is shown in figure 1. It uses a 28um substrate thickness, vias, MIM capacitors and a plated heatsink.

Power and efficiency contours derived from load pull measurements were used to determine optimum loading. The source impedances were designed to provide good gain while maintaining stability. The input is matched to 50 ohms. The output match is done externally to maintain small chip size and optimum performance. The MMIC is designed to operate optimally in the saturated region to handle signals containing constant envelope modulation such as GMSK.

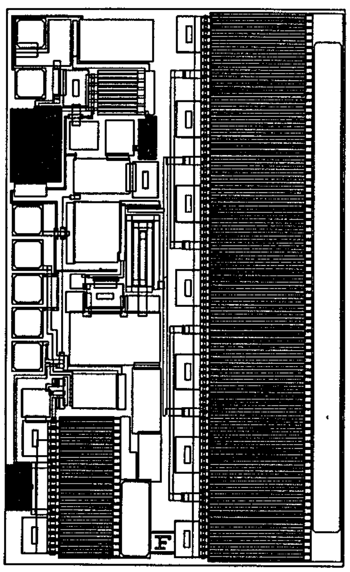

Figure 1. Chip layout

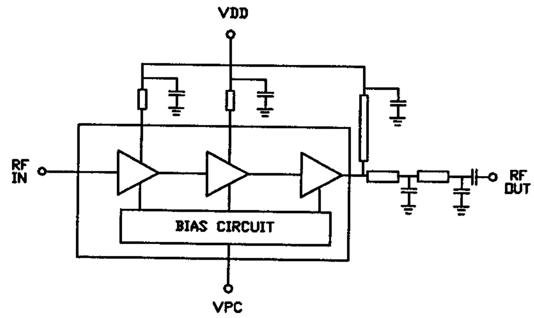


Figure 2. Block diagram

The block diagram is shown in figure 2. The output matching consists of 2 shunt capacitors along the output transmission line. The VDD3 bias stub is 20mm long on FR4 board while the VDD1 and VDD2 bias stubs are 5mm long. The VDDs are then combined and then connected directly to the battery supply. The power control voltage VPC is applied to bias up the FETs into class AB.

Power control is done by changing the VPC voltage which varies the Vgs of the three stages plus the Vds of the first stage. Power control current is under 3mA which is low enough that a driver such as an ASIC can be directly connected.

The MMIC uses a low cost, 5.5x5.0x1.1 mm plastic package with an SSOP-16 footprint. Heat sinking is done through an exposed copper alloy leadframe at the bottom of the package to provide a low thermal resistance. The outline of the package is shown in figure 3. An Rth of less than 6°C/W for a 3W device size is obtained. Low ground inductance is also achieved.

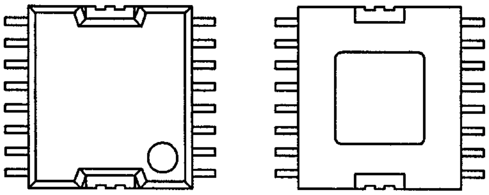

Figure 3. SSOP package outline

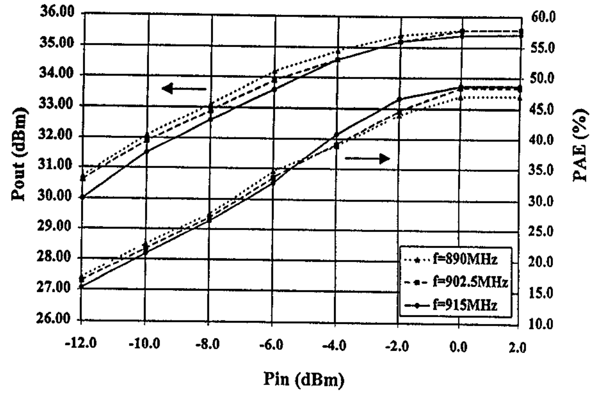


Figure 4. Pin-Pout, PAE plots

## Results

The following results are obtained in the 890-915 MHz GSM band. Pin-Pout, PAE plots are shown in figure 4. The MMIC has over 42 dB of linear gain. With Pin=0dBm and Vdd=4.8V, the output power is over 35.4 dBm with a minimum power added efficiency of 47%.

Power control characteristics are shown in figure 5 at 900 Mhz with Pin=0dBm. As the power control voltage Vpc is varied from 3V to 0V the output power goes from 35.5 dBm to -40 dBm for over 75 dB of power control range.

With Vpc=0V and no rf applied, the Ids leakage current measures 2uA. The 2nd and higher harmonics are better than -40 dBc.

Figure 6 shows performance as a function of drain voltage at 900 Mhz. At 5.7V, Pout=35.6 and PAE=50%. At 4.8V, Pout=35.5dBm and PAE=48%. At 3.6V, Pout=34.7 dBm and PAE=43%.

These results are from a first design. Further improvements in efficiency can be expected by refining the on chip matching circuits.

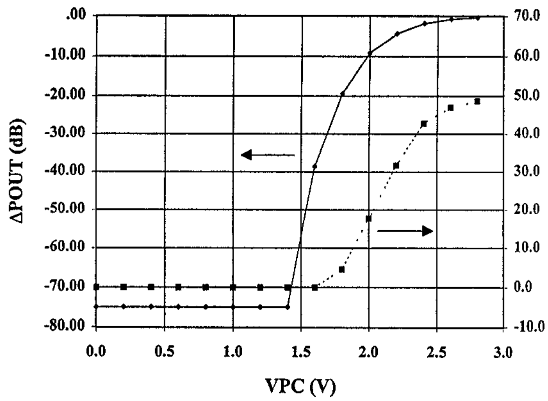


Figure 5. Power control graph, f=900MHz

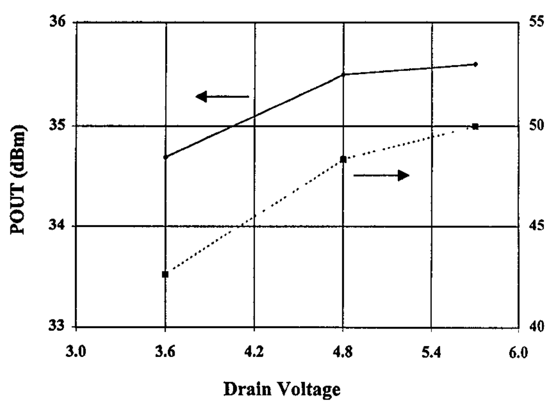


Figure 6. Pout, PAE vs. Drain Voltage

## Conclusion

We have demonstrated the performance capability of this enhancement mode MMIC for the high power requirements of the GSM band. This approach can be extended to higher frequencies and lower voltages where GaAs performance can be fully utilized. It is a reliable, low system cost solution for future wireless applications.

## Acknowledgments

The Authors would like to thank E. Mitani, K. Nanbu, T. Igarashi, H. Mochizuki, P. Gardner, S. Brozovich, L. Ton and C. Burnside for their valuable contributions.

## References

[1] E. Glass, J. Abrokwah, R. Lucero, E. Spears, J. Rollman, J. Huang, B. Bernhardt, B. Ooms, "A High Efficiency Complimentary GaAs Power FET Technology for Single Supply Portable Applications", IEEE MTT-S Digest, pp. 1083-1086, 1996.

[2] S. Nakajima, K, Matsuzaki, K. Otobe, H. Nishizawa, N. Shiga, " Enhancement Mode GaAs MESFET Technology for Low Power Consumption Power and Low Noise Applications", IEEE MTT-S Digest, pp. 1443-1446, 1994.

[3] M. Nagaoka, T. Inoue, K. Kawakyu, S. Obayashi, H. Kayano, E. Takagi, Y. Tanabe, M. Yoshimura, K. Ishida, Y. Kitaura and N. Uchitomi, "High-Efficiency Monolithic GaAs Power MESFET Amplifiers Operating with a Single Low Voltage Supply for 1.9 Ghz Digital Mobile Communications Applications", IEEE MTT-S Digest, pp. 577-580, 1994.